REMARKS/ARGUMENTS

The Applicants have carefully considered this application in connection with previous Examiner's Action and respectfully request reconsideration of this application in view of the foregoing amendment and the following remarks.

The Applicants originally submitted Claims 1-21 in the application. In the present preliminary amendment, the Applicants have amended Claims 1-2, 5, 8-9, 12, 15-16 and 19. No claims have been canceled or added. Accordingly, Claims 1-21 are currently pending in the application.

I. Rejection of Claims 1-21 under 35 U.S.C. §102

The Examiner has rejected Claims 1-21 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application No. 6,115,808 to Arora. The Applicants respectfully disagree.

Arora discloses a hazard detection circuit that includes first and second memory regions coupled to a logic circuit. The first memory region stores a predicate status vector that includes a predicate status mask bit. Each status bit of the status vector indicates whether or not its associated predicate is pending (*i.e.*, not ready) or not pending (*i.e.*, ready). (*See* column 2, lines 32-39.) Values for the predicate status vector are obtained from registers. (*See* column 3, lines 32-55.)

Arora does not, however, teach identifying and tracking conditional instructions in a wide-issue processor including causing link pointers to move through conditional link pointer register sets as recited in independent Claims 1, 8 and 15. More specifically, Arora does not disclose that each of the sets corresponds to a stage of a pipeline of the processor and cause the link pointers to move through the sets as the instructions associated with the link pointers and located in a conditional

execution block move through each of the corresponding stages of the processor as recited in amended independent Claims 1, 8 and 15. On the contrary, the Applicants do not find where Arora teaches register sets wherein each of the sets corresponds to stages of a pipeline. Additionally, the Applicants do not find where link pointers move through each of the sets as associated instructions move through corresponding pipeline stages. Instead, Arora teaches predicate vector status values that do not move through registers but remain in a single memory location. (*See* column 4, lines 57-61 and column 3, lines 32-49.) Thus, even assuming that the predicate status vector values are link pointers as recited in Claims 1, 8 and 15, Arora does not teach link point register sets wherein each set corresponds to a stage in a pipeline **nor** moving the link pointers through the sets as associated instructions move through the stages in the pipeline as presently claimed.

The Examiner states that the value of the predicate status vector changes as the instruction status changes when instructions move through the pipeline stages. Based on the value changes, the Examiner asserts that the predicate vector values effectively move through the pipeline. (*See* page 3 of the Examiner's Final Action mailed on January 24, 2005.) The Applicants respectfully disagree since a change in value of a stationary predicate status vector differs from a change in location, or more specifically, moving from one register to another register.

Accordingly, Arora does not teach each element of amended independent Claims 1, 8 and 15 and Claims dependent thereon. Thus, Arora does not anticipate Claims 1-21 and the Applicants respectfully request the Examiner to allow issuance thereof.

II. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-21.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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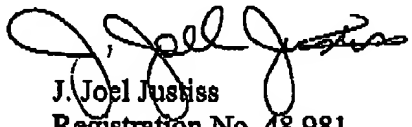

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